REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated November 17, 2003 (U.S. Patent Office Paper No. 13). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 38-42 are currently pending in this application. As outlined above, claims 18 to 27 were previously canceled without prejudice or disclaimer, while claim 38 is being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. Claims 1 to 17 and 28 to 37 currently stand withdrawn from consideration in this application.

Prior Art Rejections

Claims 38, 39, and 41 were rejected under 35 U.S.C. §102(e) as being anticipated by Liu *et al.*, U.S. Patent No. 6,211,063 B1 (further, Liu '063).

Amended claim 38 recites a method of fabricating a semiconductor integrated circuit device, comprising forming a lower layer dielectric film including a first silicon oxide film containing fluorine over a major surface of a wafer, forming an upper layer dielectric film including a second silicon oxide film substantially without fluorine as compared with the first silicon oxide film over the first oxide film, the upper and lower layer dielectric films constituting an inter-layer dielectric film having an inter-wiring layer portion and an inter-via layer portion respectively, forming via holes through said upper dielectric film and lower dielectric film and then forming wiring grooves in the upper dielectric film, wherein at least one of said wiring grooves includes one of said via holes in a groove pattern, forming a barrier metal along said wiring grooves and via holes and then filling the wiring groove and the via hole with copper so as to form an embedded wiring and a copper plug electrically connecting the embedded wiring to lower wiring, wherein Young's modulus of the lower dielectric film as a whole is smaller than that of the upper dielectric film.

The Examiner alleged in the office action on page 2 that the disclosure of figure 4, col. 4, lines 13 to 26, 46 to 57, figure 8, col. 5, line 18 to col. 6, line 10, figure 11, col. 6, lines 30 to 34 of Liu '063 anticipates claims 38, 39, and 41. Applicants respectfully disagree.

Applicants respectfully submit regarding the present invention that it is aimed to improving a via structure against damage due to thermal treatment. The metal embedded in a via tends to expand due to thermal treatment. In the present invention, the via metal expansion is released by an insulation film formed around the via metal, where the insulation film formed around the via metal has a lower Young's modulus than the insulation film formed between inter-wiring. Regarding the damascene wiring process of the present invention, the Applicants submit that as disclosed above by claim 38, it consists of the following steps: forming a lower dielectric film, forming a stopper film on the lower dielectric film, forming an upper dielectric film on the stopper film, wherein the upper dielectric film has greater Young's modulus than the lower dielectric film, forming a via hole bored through upper and lower dielectric film, forming a wiring groove in the upper dielectric film, forming barrier metal in the via hole and wiring groove, forming a copper metal on the barrier metal, and polishing out a copper and barrier metal outside the wiring groove.

Liu '063 discloses a damascene wiring process using FSG as a lower dielectric film and HSQ as an upper dielectric film. In table 4 of Liu '063, it is shown that the FSG has a larger Young's modulus than HSQ. Liu '063 discloses a damascene wiring process that consists of forming a lower dielectric film HSG and a stopper film (SiON) and patterning the stopper film, forming an upper dielectric film HSQ on the stopper film, forming wiring grooves in the upper dielectric film, forming via holes in the lower dielectric film, and embedding a cooper film in the wiring grooves and via holes.

Applicants respectfully submit that, in the present invention, the insulation film formed around via metal has a lower Young's modulus than the insulation film formed between the inter-wiring. In contrast, Liu '063 discloses a FSG as lower dielectric film with larger Young's modulus than HSQ, the upper dielectric film. The present invention contemplates a process of damascene wiring process with a step of forming a via hole bored through upper and lower dielectric film. Liu '063 discloses a damascene wiring process only through the lower dielectric film. Based on the differences outlined above, Applicants respectfully submit that Liu '063 does not anticipate the recitation of claim 38, and thereby ask the Examiner to withdraw the rejection of claim 38.

Claims 39 and 41 depend from and add features to an allowable independent claim 38. Therefore, they are also allowable for at least the same reasons discussed above in connection with claim 38.

Claim 40 is rejected under 35 U.S.C. §103(a) as being unpatentable over Liu '063 as applied to claim 38 and in further view of Huan, U.S. Patent No. 6,177,364 B1 (further, Huan '364).

Claim 40 depends from claim 38 and further adds the limitation of "the stopper film is a SiC film." Applicants respectfully submit that in light of the arguments made above in connection with claim 38, claim 40 is also allowable over Liu '063 and over any combination of Liu '063 with other references. Liu '063 does not disclose the claimed wiring process and neither does Huan '364. Therefore, although Huan '364 discloses SiC as a material for the stopper film, the combination of these references does not identically disclose, teach or suggest all the steps of the claimed wiring process. Based on the above, Applicants respectfully ask the Examiner to withdraw the rejection regarding claim 40.

Claim 42 was rejected under 35 U.S.C. §103(a) as being unpatentable over Liu '063 as applied to claim 38 and in further view of Komada, U.S. Patent No. 6,627,554 B1 (further, Komada '554).

Claim 42 recites a method of fabricating a semiconductor integrated circuit device according to claim 38, wherein a stopper dielectric film is not formed between the inter-wiring layer portion and the inter-via layer portion.

In response to the above rejection Applicants respectfully submit that Komada '554 discloses a tungsten via and copper single damascene wiring in Fig. 3. Fig. 3 illustrates a tungsten plug 7 and cooper damascene wiring 12. The wiring groove and the via hole is not formed at the same time as forming a barrier metal and copper metal along a surface of the groove and via, as described in col. 4, line 63 through col. 5, line 18. Applicants also submit that claim 42 depends from and adds features to an allowable claim 38. Based on the above, Applicants respectfully submit that claim 42 is allowable over any combination of the above references and respectfully ask the Examiner to withdraw the rejection of claim 42.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

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